AMENDMENTS TO THE SPECIFICATION:

Page 3, replace the paragraph, beginning on line 12, bridging pages 3 and 4, with the following amended paragraph:

--Then, semiconductor chip 4 on which bumps 5 are formed is adsorbed and held by chip mounting tool 18 that has adsorption hole 19, and semiconductor chip 4 is aligned with wiring on the wiring substrate. Successively, as shown in FIG. 2B, chip mounting tool 18 is moved down to make bumps 5 come into contact with wiring pattern 2 while semiconductor chip 4 is adsorbed and held. While this state is maintained, heat and pressure are applied to semiconductor chip 4 to connect the bumps and the wiring and to harden the resin between the semiconductor chip and the wiring substrate, thereby forming underfill 17. In the second conventional example, although expansion of the substrate by heat during mounting has not changed, stress, which is generated due to contraction of the substrate when it returns to room temperature, is dispersed over underfill 17. Therefore, it is possible to prevent to poor connection caused by the difference between thermal expansion coefficients of the semiconductor chip and the wiring substrate, that is, the problem in the above-described technique where the resin is injected and hardened after mounting. Further, this example is provided with the feature in which low-temperature connection is available only by contact of bumps 5 and the wiring on the wiring substrate. However, in recent years, demand for use in ~~potable~~ portable terminal devices has become

severe, and it has become essential to manufacture discrete semiconductor chips that have thin profiles. A significant problem emerges in which resin climbs the chip mounting tool of the semiconductor chip mounting device while the chip is being mounted in the case of thin chips, and resin adheres to the tool.-

Page 5, replace the paragraph, beginning on line 20, bridging pages 5 and 6, with the following amended paragraph:

--Also, FIGs. 4A and 4B show an example in which semiconductor chips are laminated and BGA (ball grid array) is manufactured according to the conventional mounting method. FIG. 4A is a plan view of the wiring layer of an uppermost layer, and FIG. 4B is a cross-sectional view of a conventional BGA. Similarly, to the example shown in FIGs. 3A and 3B, bumps for semiconductor chip 4 are drawn out to via hole land 21 through pad 20 and through wiring patterns 2 formed in the uppermost wiring layer, and fall to the lower wiring layer. Pads 23 for wire bonding are formed on the peripheral portion of insulating layer 12 of the uppermost layer. On semiconductor chip 4, another semiconductor chip 16 is mounted in a face-up state. Electrodes (not shown) of another semiconductor chip 16 and pads 23 are connected with bonding wires [[23]] 24.--